Questions/Comments Regarding JPL D-25647 DEWAR Subsystem Specification Dated 12 March 2004 28 April 2004

3.2.4.3.6 Self-Induced Shock Testing

Testing for self induced shock shall be performed by operating any shock-inducing devices a minimum of two times.

Question:

Would an externally imposed shock test (2x) be an acceptable alternative?

Answer:

In work. Yes, an externally imposed shock test (2x) is an acceptable alternative providing that the shock characteristics closely mimic the shock-inducing-device frequency spectrum, and that the force(s) are applied at the identical shock-inducing-device location.

3.2.5.2.1 Abnormal Input Voltage

The Dewar Control Electronics shall survive steady-state voltages in the range 0 V dc to 36 V dc and momentary (no greater than 10 ms) voltages in the range 0 V dc to 42 V dc.

Question:

Paragraph 3 2.3.3.1.8 defines a steady state input voltage of 40 volts over-voltage, yet in this paragraph defines a voltage of 42 volts as an over-voltage value. Which is the real requirement, or why are they different?

Answer:

In work. Replace 3.2.5.2.1 Abnormal Input Voltage, as follows: 3.2.5.2.1 (Intentionally left blank); and delete the following:

The Dewar Control Electronics shall survive steady-state voltages in the range 0V dc to 36 V dc and momentary (no greater than 10 ms) voltages in the range 0 V dc to 42 V dc.

3.2.5.2.3 (left blank)

Ouestion:

This clock signal interface does not show on Figure 1.3-1, and in fact is not needed in our proposed operational concept of the DCE. Where is the requirement for this clock synchronization?

Answer:

The requirement associated with 3.2.5.2.3 should be deleted. Replace 3.2.5.2.3 Unannounce Clock Signal Loss, as follows: 3.2.5.2.3 (Intentionally left blank); and delete the following:

The Dewar Control Electronics shall meet the performance rquirements of this specification after experiencing the unannounced removal and arbitrary reconnection of the external synchronization clock signal.